METHOD OF HANDLING BRANCHING INSTRUCTIONS WITHIN A PROCESSOR, IN PARTICULAR A PROCESSOR FOR DIGITAL SIGNAL PROCESSING, AND CORRESPONDING PROCESSOR

Abstract of the Disclosure

A processor includes a program memory containing program instructions, and a processor core including several processing units and a central unit. The central unit, upon receipt of a program instruction, issues corresponding instructions to the various processing units. The processor core is clocked by a clock signal. A branching instruction received by the central unit, in the course of a current cycle, is processed in the course of the current cycle.